R15

Code No: 124AF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, February - 2024
DIGITAL DESIGN USING VERILOG HDL
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART - A

(25 Marks)

1.a)	What are system tasks in Verilog?	[2]
b)	Briefly describe the difference between simulation and synthesis in Verilog.	[3]
c)	Define the basic function of an AND gate primitive.	[2]
d)	How can gate primitives be utilized in the design of flip-flops?	[3]
e)	Define functional bifurcation and its role in behavioral models.	[2]
f)	Differentiate between operations and assignments in the context of Behavioral Modeling.	[3]
g)	What are module parameters in Verilog?	[2]
h)	What is the role of parameters in system tasks and functions?	[3]
i)	Briefly explain capacitive model.	[2]
j)	Write Verilog code using Case statement.	[3]

PART - B

(50 Marks)

2.a) Explain in detail about the unary, binary and ternary operators in Verilog with examples.
b) Describe about white space characters and variables in Verilog HDL. [5+5]

OR

3.a) Explain the role of operators in Verilog HDL. Discuss various types of operators, their precedence, and how they are utilized in the manipulation of data in Verilog code.
b) Explore the concept of parameters in Verilog HDL. Discuss their significance in design parameterization, configuration management. [5+5]

4.a) Write Verilog module for a positive edge triggered flip flop with test bench.
b) What are tri-state devices? Write a Verilog code for tri-state devices. [5+5]

OR

5.a) With an example explain in detail about the use of gate primitives in the design of complex digital circuits.
b) Describe the role of flip-flops in sequential logic circuits and their significance in digital systems. [5+5]

6.a) Explain the functionality and purpose of the 'wait' construct in behavioral modeling.
b) Explain the concept of multiple 'always' blocks in behavioral modeling. [5+5]

OR

7.a) Explain in detail about the functionality and syntax of the 'case' statement in behavioral modeling.

b) Describe the simulation flow when using 'if' and 'if-else' constructs in behavioral modeling. [5+5]

8. Explain how path delays are modeled and their role in ensuring accurate simulation results. [10]

OR

9.a) Explain the concept of instantiation in Verilog? Discuss how instantiation parameters influence the behavior and performance of instantiated components.

b) Explain the concept of hierarchical access in Verilog and discuss its importance in organizing and managing complex designs. [5+5]

10.a) Explain the concept of the implicit model in sequential circuits. Discuss how it differs from other sequential models.

b) Briefly explain any one method used for sequential circuit testing. [5+5]

OR

11.a) Explain in detail about formal verification of a system.

b) Describe the techniques employed in creating an effective test bench for sequential circuit testing. [5+5]

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